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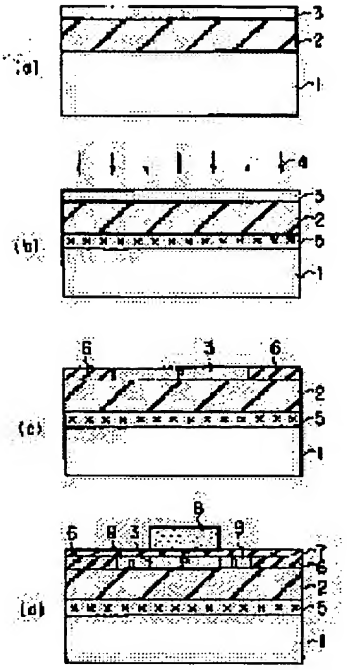
(54) SEMICONDUCTOR DEVICE AND ITS MANUFACTURE

(57)Abstract:
PROBLEM TO BE SOLVED: To form a strained silicon layer through a simple method without generating dislocation defects.
SOLUTION: A first silicon layer 1, an SiO2 layer 2, and a second silicon layer 3 are successively laminated for the formation of an SOI substrate, ions 4 are implanted into the first silicon layer 1, a dislocation defect region 5 is formed inside the first silicon layer 1 through a first annealing process, the first silicon layer 1 and the SiO2 layer 2 are separated from each other in terms of stress, and a tensile strain is induced in the second silicon layer 2 through a second annealing process carried out at least at the viscous fluid temperature of SiO2.



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* NOTICES *

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CLAIMS

[Claim(s)]
[Claim 1] The semiconductor device characterized by having come to provide the substrate with which it comes to carry out the laminating of the 1st semi-conductor layer, an insulating layer, and the 2nd semi-conductor layer one by one, and for distortion being contained in said 2nd semi-conductor layer, and forming the component.
[Claim 2] The semiconductor device according to claim 1 characterized by forming the rearrangement defective field in said 1st semi-conductor layer.
[Claim 3] Said rearrangement defective field is a semiconductor device according to claim 2 characterized by being formed in the interface of said 1st semi-conductor layer and said insulating layer.
[Claim 4] Said 1st semi-conductor layer uses silicon as a principal component, and the consistency of the rearrangement defect of said rearrangement defective field is 2 1x1010 pieces/cm. Semiconductor device according to claim 2 or 3 characterized by being above.
[Claim 5] The semiconductor device according to claim 1 to 4 with which thickness of said 2nd semi-conductor layer is characterized by being smaller than said insulating layer thickness.
[Claim 6] Said 2nd semi-conductor layer is a semiconductor device according to claim 1 to 4 which uses silicon as a principal component and is characterized by said distortion being hauling distortion from which the lattice constant of said silicon in said 2nd semi-conductor layer becomes 1.01 or more times of the original lattice constant of silicon.
[Claim 7] Said 2nd semi-conductor layer uses silicon as a principal component, and said insulating layer is SiO2. Semiconductor device according to claim 1 to 4 with which it considers as a principal component, and thickness of said 2nd semi-conductor layer is characterized by being 1/5 or less [of said insulating layer thickness].
[Claim 8] By the process which the 1st semi-conductor layer, an insulating layer, and the 2nd semi-conductor layer prepare the substrate which comes to carry out a laminating one by one, and injects ion into said 1st semi-conductor layer, and heat treatment While forming the rearrangement defective field based on said ion in said 1st semi-conductor layer and separating said the 1st semi-conductor layer and said insulating layer in stress The manufacture approach of the semiconductor device characterized by having the process which makes said 2nd semi-conductor layer generate distortion, and the process which forms a component in said 2nd semi-conductor layer.
[Claim 9] Said heat treatment is the manufacture approach of the semiconductor device according to claim 8 which carries out the description of consisting of the 1st heat treatment which forms said rearrangement defective field, and the 2nd heat treatment which it is carried [heat treatment] out after this 1st heat treatment, and generates said distortion.
[Claim 10] The temperature of said 2nd heat treatment is the manufacture approach of the semiconductor device according to claim 9 which carries out the description of being beyond the viscous flow temperature of said insulating layer.
[Claim 11] Said insulating layer is SiO2. It is the manufacture approach of the semiconductor device according to claim 10 which considers as a principal component and carries out the description of said temperature being 900 degrees C or more.

[Claim 12] Said heat treatment is the manufacture approach of the semiconductor device according to claim 8 characterized by being what performs formation of said rearrangement defective field, and induction of said distortion to coincidence.
[Claim 13] Said ion is the manufacture approach of the semiconductor device according to claim 8 to 12 characterized by being the ion of at least one element chosen from the element group which consists of a hydrogen element and an inactive element.

[Translation done.]

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] This invention relates to the semiconductor device which formed the component in the semi-conductor layer containing distortion, and its manufacture approach.
[0002]
[Description of the Prior Art] Many transistors, resistance, etc. are connected to the important parts of a computer or communication equipment so that an electrical circuit may be attained, and the large-scale integrated circuit (LSI) integrated and formed on 1 chip is used abundantly. For this reason, the engine performance of the whole device is connected as greatly as the engine performance of an LSI simple substance.
[0003] In the improvement in the engine performance of the LSI simple substance which consists of improvement in the engine performance of an LSI simple substance, for example, an Si system MOS device etc., implementation of MOSFET characterized by the high speed and the low power is indispensable. For this reason, for example, researches and developments aiming at improvement in electrical characteristics, such as current driving force, are done energetically.
[0004] The technique which forms a component in the silicon layer (distortion silicon layer) containing distortion as one of the techniques for heightening current driving force is known. The sectional view of the substrate which has the conventional distortion silicon layer in drawing 3 is shown.
[0005] Among drawing, 81 show the silicon substrate and sequential formation of the gray TEDDO SiGe mixed-crystal layer 82, the relaxation SiGe mixed-crystal layer 83, and the distortion silicon layer 84 is carried out on this silicon substrate 81. In this kind of substrate, a rearrangement defect is shut up in the gray TEDDO SiGe mixed-crystal layer 82, and it is supposed that a rearrangement defect will not go into the relaxation SiGe mixed-crystal layer 83.

[0006]
[Problem(s) to be Solved by the Invention] However, in fact, a rearrangement defect will go even into the relaxation SiGe mixed-crystal layer 83, and this rearrangement defect will reach even the distortion silicon layer 84 further. Therefore, since the dependability of the distortion silicon layer 84 fell, even if it formed the component in the distortion silicon layer 84 according to this rearrangement defect, there was a problem that it was difficult to acquire the electrical characteristics as expected.
[0007] Furthermore, since the highly precise epitaxial growth system and the process technique were required in order to form the gray TEDDO SiGe mixed-crystal layer 82 and the relaxation SiGe mixed-crystal layer 83, there was a problem that it was difficult to form the distortion silicon layer 84 easily.
[0008] Although the distortion silicon layer was effective in improvement in component properties, such as current driving force, like ****, there was a problem that it was difficult to form easily without causing generating of a rearrangement defect.
[0009] This invention was made in consideration of the above-mentioned situation, and the place made into the purpose is to offer the semiconductor device equipped with the substrate which

can be formed easily, and its manufacture approach, without inviting generating of a rearrangement defect for this distortion semi-conductor layer to the interior, including a distortion semi-conductor layer.
[0010]
[Means for Solving the Problem]
[Summary of the Invention] -- in order to attain the account purpose of a top, the semiconductor device (claim 1) concerning this invention is characterized by having come to provide the substrate with which it comes to carry out the laminating of the 1st semi-conductor layer, an insulating layer, and the 2nd semi-conductor layer one by one, and for distortion being contained in said 2nd semi-conductor layer, and forming the component.
[0011] Moreover, other semiconductor devices (claim 2) concerning this invention are characterized by forming the rearrangement defective field in said 1st semi-conductor layer in the above-mentioned semiconductor device (claim 1).
[0012] Moreover, other semiconductor devices (claim 3) concerning this invention are characterized by forming said rearrangement defective field in the interface of said 1st semi-conductor layer and said insulating layer in the above-mentioned semiconductor device (claim 2).

[0013] Moreover, for other semiconductor devices (claim 4) concerning this invention, in the above-mentioned semiconductor device (claim 2, claim 3), said 1st semi-conductor layer uses silicon as a principal component, and the consistency of the rearrangement defect of said rearrangement defective field is 2 1x1010 pieces/cm. It is characterized by being above.
[0014] Moreover, it is characterized by other semiconductor devices (claim 5) concerning this invention having the thickness of said 2nd semi-conductor layer smaller than said insulating layer thickness in the above-mentioned semiconductor device (claim 1 - claim 4).
[0015] Moreover, in the above-mentioned semiconductor device (claim 1 - claim 4), said 2nd semi-conductor layer uses silicon as a principal component, and other semiconductor devices (claim 6) concerning this invention are characterized by the lattice constant of said silicon [distortion / said] in said 2nd semi-conductor layer being hauling distortion used as 1.01 or more times of the original lattice constant of silicon.
[0016] Moreover, for other semiconductor devices (claim 7) concerning this invention, in the above-mentioned semiconductor device (claim 1 - claim 4), said 2nd semi-conductor layer uses silicon as a principal component, and said insulating layer is SiO2. It considers as a principal component and thickness of said 2nd semi-conductor layer is characterized by being 1/5 or less [of said insulating layer thickness].
[0017] Moreover, the manufacture approach (claim 8) of the semiconductor device concerning this invention By the process which the 1st semi-conductor layer, an insulating layer, and the 2nd semi-conductor layer prepare the substrate which comes to carry out a laminating one by one, and injects ion into said 1st semi-conductor layer, and heat treatment While forming the rearrangement defective field based on said ion in said 1st semi-conductor layer and separating said the 1st semi-conductor layer and said insulating layer in stress, it is characterized by having the process which makes said 2nd semi-conductor layer generate distortion, and the process which forms a component in said 2nd semi-conductor layer.
[0018] Moreover, the manufacture approach (claim 9) of other semiconductor devices concerning this invention is performed in the manufacture approach (claim 8) of the above-mentioned semiconductor device after the 1st heat treatment in which said heat treatment forms said rearrangement defective field, and this 1st heat treatment, and the description of consisting of the 2nd heat treatment which generates said distortion is carried out.
[0019] Moreover, the manufacture approach (claim 10) of other semiconductor devices concerning this invention carries out the description of the temperature of said 2nd heat treatment being beyond the viscous flow temperature of said insulating layer in the manufacture approach (claim 9) of the above-mentioned semiconductor device.
[0020] Moreover, for the manufacture approach (claim 11) of other semiconductor devices concerning this invention, it sets to the manufacture approach (claim 10) of the above-mentioned semiconductor device, and said insulating layer is SiO2. It considers as a principal

component and the description of said temperature being 900 degrees C or more is carried out.
[0021] Moreover, the manufacture approach (claim 12) of other semiconductor devices concerning this invention is characterized by said heat treatment being what performs formation of said rearrangement defective field, and induction of said distortion to coincidence in the manufacture approach (claim 8) of the above-mentioned semiconductor device.
[0022] Moreover, the manufacture approach (claim 13) of other semiconductor devices concerning this invention is characterized by being the ion of at least one element chosen from the element group which said ion becomes from a hydrogen element and an inactive element in the manufacture approach (claim 8 - claim 12) of the above-mentioned semiconductor device.
[0023] A base [operation] this invention view has the 1st semi-conductor layer, an insulating layer, and the 2nd semi-conductor layer in using the substrate (SOI substrate) which comes to carry out a laminating one by one, in order to obtain a distortion semi-conductor layer.
[0024] That is, in this invention, first, ion is injected into the 1st semi-conductor layer, and a rearrangement defective field is formed in the 1st semi-conductor layer by heat treatment. A rearrangement defective field can separate the 1st semi-conductor layer and insulating layer in stress.
[0025] Thus, if the 1st semi-conductor layer and insulating layer lower the 2nd semi-conductor layer and insulating layer to a room temperature from a hot (preferably beyond the viscous flow temperature of an insulating layer) condition in the condition of having dissociated in stress, the 2nd semi-conductor layer and insulating layer will come to receive distortion decided by both coefficient of thermal expansion and thickness.
[0026] Here, although a coefficient of thermal expansion is unchangeable, since thickness is changeable, sufficient distortion for the 2nd semi-conductor layer can be generated by adjusting the 2nd semi-conductor layer and insulating layer thickness.
[0027] Thus, according to this invention, sufficient hauling distortion for the 2nd semi-conductor layer can be produced by the ion implantation and heat treatment. Namely, a distortion semi-conductor layer can be easily formed now, without using a highly precise epitaxial growth system and a process technique.
[0028] Moreover, in this invention, although a rearrangement defective field is formed, since the insulating layer dissociates with the 2nd semi-conductor layer, a rearrangement defect does not generate this rearrangement defective field in the 2nd semi-conductor layer. Namely, a reliable distortion semi-conductor layer can be formed now.
[0029] Therefore, according to this invention, it can be reliable and the semi-conductor layer which has sufficient hauling distortion can be easily formed now. The semiconductor device (claim 1) concerning this invention is the thing of most fundamental configuration of that offer of a reliable distortion semi-conductor layer is attained.
[0030] Moreover, the characteristic configuration (rearrangement defective field) produced in case the semiconductor device (claim 2) concerning this invention manufactures the above-mentioned semiconductor device (claim 1) is added. Moreover, the semiconductor device (claim 3) concerning this invention limits the location of the most desirable rearrangement defective field, in order to obtain sufficient distortion.
[0031] Moreover, the semiconductor device (claim 4) concerning this invention limits the typical value of a rearrangement defective field in case the principal component of the 1st semi-conductor layer is silicon. Moreover, the semiconductor device (claim 5) concerning this invention limits the size relation between the thickness of the 2nd semi-conductor layer effective in obtaining sufficient distortion, and that of an insulating layer.
[0032] moreover, the case where the principal component of the 2nd semi-conductor layer of the semiconductor device (claim 6) concerning this invention is silicon -- this -- the value of the typical tensile stress, from which the 2nd semi-conductor layer is obtained is limited.
[0033] Moreover, for the principal component of the 2nd semi-conductor layer, the principal component of silicon and an insulating layer is [the semiconductor device (claim 7) concerning this invention] SiO2. The size relation between the thickness of the 2nd semi-conductor layer effective in obtaining sufficient distortion and that of an insulating layer is limited to a case.
[0034] Moreover, the manufacture approach (claim 8) of the semiconductor device concerning

this invention is the thing of most fundamental configuration of that offer of a reliable distortion semi-conductor layer is attained. Moreover, the manufacture approach (claim 9) of the semiconductor device concerning this invention limits having divided into the 1st heat treatment for forming a rearrangement defective field for heat treatment, and the 2nd heat treatment for making the 2nd semi-conductor layer generate distortion in the manufacture approach (claim 8) of the above-mentioned semiconductor device.

[0035] Moreover, the manufacture approach (claim 10) of the semiconductor device concerning this invention limits the desirable temperature of the 2nd heat treatment. Moreover, for the manufacture approach (claim 11) of the semiconductor device concerning this invention, the principal component of an insulating layer is SiO2. The desirable temperature of the 2nd heat treatment of a case is limited.

[0036] Moreover, the manufacture approach (claim 12) of the semiconductor device concerning this invention limits managing one heat treatment in the manufacture approach (claim 8) of the above-mentioned semiconductor device, without dividing into heat treatment for forming a rearrangement defective field, and heat treatment for making the 2nd semi-conductor layer generate distortion. Moreover, the manufacture approach (claim 13) of the semiconductor device concerning this invention limits ion effective in forming a rearrangement defective field.

[0037]

[Embodiment of the Invention] Hereafter, the gestalt (henceforth an operation gestalt) of operation of this invention is explained, referring to a drawing.

(1st operation gestalt) Drawing 1 </A> is the process sectional view showing the formation approach of MOSFET concerning the 1st operation gestalt of this invention .

[0038] First, as shown in drawing 1 (a), they are the 1st silicon layer 1 as a support substrate, and SiO2. A layer 2 and the 2nd silicon layer 3 as a barrier layer in which a component is formed prepare the SOI substrate which comes to carry out a laminating one by one.

[0039] The thickness of the 1st silicon layer 1 is 700 micrometers and SiO2. The thickness of 100 micrometers and the 2nd silicon layer 3 of the thickness of a layer 2 is 20 micrometers. Thus, for the usual SOI substrate, the SOI substrates of this operation gestalt differ and the 2nd silicon layer 3 is SiO2. It is thinner than a layer 2. This is for heightening the effectiveness of this invention mentioned later. The thickness of the 2nd silicon layer 3 is SiO2 like this operation gestalt. It is desirable that it is 1/5 or less [of the thickness of a layer 2].

[0040] As the formation approach of a SOI substrate, after injecting oxygen ion into a silicon layer, any usual approach, such as the approach (SIMOX law) of performing annealing and forming a silicon oxidizing zone and the approach (lamination method) of making the silicon layer of two sheets rival through a silicon oxidizing zone, and forming it, may be used.

[0041] Next, as shown in drawing 1 (b), it is 2 acceleration voltage 20keV and 1x1016 doses/cm. On conditions, a hydrogen ion is injected into the 1st silicon layer 1 from the 2nd silicon layer 3 side. Thereby, a hydrogen ion is the 1st silicon layer 1 and SiO2. It is introduced into the 1st silicon layer [/ near the interface with a layer 2] 1.

[0042] In addition, the ion of an inactive element may be poured in instead of a hydrogen ion. As ion, a hydrogen ion and the ion of an inactive element are used because these ion is effective in formation of a rearrangement defect.

[0043] Next, as shown in this drawing (b), the 1st annealing with a temperature of about 400-600 degrees C is performed, and it is the 1st silicon layer 1 and SiO2. In the 1st [near the interface with a layer 2] silicon layer 1, the consistency of a rearrangement defect is 2 about 1x1015 pieces/cm. The rearrangement defective field 5 is formed. By this rearrangement defective field 5, it is the 1st silicon layer 1 and SiO2. It dissociates in [a layer 2] stress.

[0044] The consistency of the defect is small and seems in addition, not to form a defective field like this operation gestalt in the usual SOI substrate, although a defect exists in the silicon layer by the side of an insulator layer.

[0045] Then, SiO2 The 2nd with a viscous flow temperature [of a layer 2 / beyond] (900 degrees C), for example, about 950-degree C temperature, annealing is performed, it pulls in the 2nd silicon layer 3, and distortion is generated. The SOI substrate which pulls in this phase and has distortion is completed.

[0046] The reason which pulls in the 2nd silicon layer 3 and distortion generates is as follows. SiO2 Above the viscous flow temperature of a layer 2, it is SiO2. The stress of a layer 2 and the 2nd silicon layer 3 is eased.
[0047] and -- if temperature falls even from the high temperature beyond viscous flow temperature to a room temperature -- SiO two-layer -- the 2 and 2nd silicon layers 3 will take charge of distortion decided by both coefficient of thermal expansion and thickness, respectively.

[0048] Specifically, it is SiO2. Since a coefficient of thermal expansion is 4.0x10-6/degree C, 0.4x10-6/degree C and the number of thermal-expansion formation of silicon For example, SiO2 Hauling distortion from which the thickness of a layer 2 will become 1.01 or more times of the lattice constant of original [lattice constant / of the silicon in the 2nd silicon layer 3] of silicon if the thickness of 100nm and the 2nd silicon layer 3 is 20nm occurs in the 2nd silicon layer 3.
[0049] Generally hauling distortion generated in the 2nd silicon layer 3 is SiO2. It becomes so large that the 2nd silicon layer 3 is so thin that the thickness of a layer 2 is thick. Then, in order to generate tensile stress sufficient with this operation gestalt for the 2nd silicon layer 3, as it mentioned above, the usual SOI substrates differ, and it is the thickness of the 2nd silicon layer 3 SiO2 It is made smaller than that of a layer 2.
[0050] To Table 1, it is SiO2. The value of the hauling distortion in the thickness (Si thickness) of the 2nd typical silicon layer 3 in case the thickness of a layer 2 is 100nm is shown. The percentage to an original lattice constant has shown hauling distortion. The thickness of the 2nd silicon layer 3 is SiO2 from a table. About [of the thickness of a layer 2 / 1/5 or less], it turns out that sufficient hauling distortion of about 1% is obtained.
[0051]
[Table 1]

Si膜厚 (mm)	引っ張り歪み (%)
100	0.032
80	0.035
60	0.042
40	0.062
20	0.117

(SiO_2 膜厚：100nm)

[0052] Here, if the rearrangement defective field 5 does not exist that is, it is the 1st silicon layer 1 and SiO2. If the layer 2 is not separated in stress, since the 1st silicon layer 1 of overwhelming thickness (700 micrometers) will govern the whole, it is SiO2. Although a layer 2 receives a big distortion, the 2nd silicon layer 2 hardly receives distortion.
[0053] In addition, you may make it the 1st annealing serve as the 2nd annealing by making temperature of the 1st annealing into 950 degrees C. Next, as shown in drawing 1 (c), isolation is performed by processing the 2nd silicon layer 3 into island shape, and embedding and forming the isolation insulator layer 6 in the perimeter. Next, as shown in this drawing (c), p mold impurity is introduced into the 2nd silicon layer 3, and a threshold electrical potential difference is adjusted.
[0054] Next, as shown in drawing 1 (d), after forming gate oxide 7 in the whole surface, the gate electrode 8 which consists of polycrystalline silicon is formed. Finally, by the ion implantation of n mold impurity which used the gate electrode 8 for the mask, the source drain diffusion layer 9 is formed in self align, and basic structure is completed.
[0055] After this, processes, such as a deposition process of an interlayer insulation film, a puncturing process of a contact hole, and a formation process of a source drain electrode, as well as the process of the usual MOSFET continue.
[0056] As stated above, according to the formation approach of this operation gestalt, sufficient hauling distortion for the 2nd silicon layer 3 can be produced by the ion implantation in the process of drawing 1 (b), and annealing of the 1st and 2 **. Namely, a distortion silicon layer can be easily formed now, without using a highly precise epitaxial growth system and a process

technique.
[0057] Moreover, although the rearrangement defective field 5 is formed by the formation approach of this operation gestalt, this rearrangement defective field 5 is SiO2. By the layer 2, since it dissociates in the 2nd silicon layer 3, a rearrangement defect does not occur in the 2nd silicon layer 3. Namely, a reliable distortion silicon layer can be formed now.
[0058] Therefore, according to this operation gestalt, it can be reliable and the silicon layer 3 which has sufficient hauling distortion can be easily formed now. Moreover, a channel is formed in the silicon layer 3 which has sufficient hauling distortion in MOSFET of this operation gestalt. Generally, in the large distortion silicon layer of hauling distortion, an electronic effective mass becomes small.
[0059] Therefore, according to this operation gestalt, high MOSFET of current drive capacity can be realized now. For example, if the large distortion silicon layer of hauling distortion is used, compared with the case where an undistorted silicon layer is used, the component of the current drive capacity to be twice [about] many as this is realizable as reported to "International Electron Device Conference 1944 proceedings."
[0060] Moreover, as mentioned above, since the dependability without a rearrangement defect of the silicon layer 3 (component formation field) is high, only high current drive capacity is not only realizable, but it can realize stable high current drive capacity.
[0061] In addition, this invention is not limited to the above-mentioned operation gestalt. For example, although the above-mentioned operation gestalt explained the case where this invention was applied to MOSFET, this invention is applicable to other semiconductor devices, for example, a bipolar transistor. The sectional view of the bipolar transistor which applied this invention to drawing 2 is shown. Among drawing, in 11, n mold collector layer and 12 show p mold base layer, and 13 shows n mold emitter layer.
[0062] Moreover, since current drive capacity is high, semiconductor devices which applied this invention, such as MOSFET and a bipolar transistor, are effective as a configuration component of a logical circuit, for example.
[0063] moreover -- the above-mentioned operation gestalt -- the principal component of a semi-conductor layer -- the principal component of silicon and an insulating layer -- SiO2 it is -- although the case where it was a SOI substrate was explained, this invention is applicable also to the SOI (Semiconductor On Insulator) substrate of other ingredient systems. In addition, in the technical range of this invention, it deforms variously and can carry out.
[0064]
[Effect of the Invention] As stated above, according to this invention, a distortion silicon layer without a rearrangement defect can be easily obtained now by using the substrate (SOI substrate) with which it comes to carry out the laminating of the 1st semi-conductor layer, an insulating layer, and the 2nd semi-conductor layer one by one.

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TECHNICAL PROBLEM

[Problem(s) to be Solved by the Invention] However, in fact, a rearrangement defect will go even into the relaxation SiGe mixed-crystal layer 83, and this rearrangement defect will reach even the distortion silicon layer 84 further. Therefore, since the dependability of the distortion silicon layer 84 fell, even if it formed the component in the distortion silicon layer 84 according to this rearrangement defect, there was a problem that it was difficult to acquire the electrical characteristics as expected.
[0007] Furthermore, since the highly precise epitaxial growth system and the process technique were required in order to form the gray TEDDO SiGe mixed-crystal layer 82 and the relaxation SiGe mixed-crystal layer 83, there was a problem that it was difficult to form the distortion silicon layer 84 easily.
[0008] Although the distortion silicon layer was effective in improvement in component properties, such as current driving force, like ****, there was a problem that it was difficult to form easily without causing generating of a rearrangement defect.
[0009] This invention was made in consideration of the above-mentioned situation, and the place made into the purpose is to offer the semiconductor device equipped with the substrate which can be formed easily, and its manufacture approach, without inviting generating of a rearrangement defect for this distortion semi-conductor layer to the interior, including a distortion semi-conductor layer.

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MEANS

[Means for Solving the Problem]
[Summary of the Invention] -- in order to attain the account purpose of a top, the semiconductor device (claim 1) concerning this invention is characterized by having come to provide the substrate with which it comes to carry out the laminating of the 1st semi-conductor layer, an insulating layer, and the 2nd semi-conductor layer one by one, and for distortion being contained in said 2nd semi-conductor layer, and forming the component.
[0011] Moreover, other semiconductor devices (claim 2) concerning this invention are characterized by forming the rearrangement defective field in said 1st semi-conductor layer in the above-mentioned semiconductor device (claim 1).
[0012] Moreover, other semiconductor devices (claim 3) concerning this invention are characterized by forming said rearrangement defective field in the interface of said 1st semi-conductor layer and said insulating layer in the above-mentioned semiconductor device (claim 2).

[0013] Moreover, for other semiconductor devices (claim 4) concerning this invention, in the above-mentioned semiconductor device (claim 2, claim 3), said 1st semi-conductor layer uses silicon as a principal component, and the consistency of the rearrangement defect of said rearrangement defective field is 2 1x1010 pieces/cm. It is characterized by being above.
[0014] Moreover, it is characterized by other semiconductor devices (claim 5) concerning this invention having the thickness of said 2nd semi-conductor layer smaller than said insulating layer thickness in the above-mentioned semiconductor device (claim 1 - claim 4).
[0015] Moreover, in the above-mentioned semiconductor device (claim 1 - claim 4), said 2nd semi-conductor layer uses silicon as a principal component, and other semiconductor devices (claim 6) concerning this invention are characterized by the lattice constant of said silicon [distortion / said] in said 2nd semi-conductor layer being hauling distortion used as 1.01 or more times of the original lattice constant of silicon.
[0016] Moreover, for other semiconductor devices (claim 7) concerning this invention, in the above-mentioned semiconductor device (claim 1 - claim 4), said 2nd semi-conductor layer uses silicon as a principal component, and said insulating layer is SiO2. It considers as a principal component and thickness of said 2nd semi-conductor layer is characterized by being 1/5 or less [of said insulating layer thickness].
[0017] Moreover, the manufacture approach (claim 8) of the semiconductor device concerning this invention By the process which the 1st semi-conductor layer, an insulating layer, and the 2nd semi-conductor layer prepare the substrate which comes to carry out a laminating one by one, and injects ion into said 1st semi-conductor layer, and heat treatment While forming the rearrangement defective field based on said ion in said 1st semi-conductor layer and separating said the 1st semi-conductor layer and said insulating layer in stress, it is characterized by having the process which makes said 2nd semi-conductor layer generate distortion, and the process which forms a component in said 2nd semi-conductor layer.
[0018] Moreover, the manufacture approach (claim 9) of other semiconductor devices concerning this invention is performed in the manufacture approach (claim 8) of the above-mentioned semiconductor device after the 1st heat treatment in which said heat treatment forms said

rearrangement defective field, and this 1st heat treatment, and the description of consisting of the 2nd heat treatment which generates said distortion is carried out.
[0019] Moreover, the manufacture approach (claim 10) of other semiconductor devices concerning this invention carries out the description of the temperature of said 2nd heat treatment being beyond the viscous flow temperature of said insulating layer in the manufacture approach (claim 9) of the above-mentioned semiconductor device.
[0020] Moreover, for the manufacture approach (claim 11) of other semiconductor devices concerning this invention, it sets to the manufacture approach (claim 10) of the above-mentioned semiconductor device, and said insulating layer is SiO2. It considers as a principal component and the description of said temperature being 900 degrees C or more is carried out.
[0021] Moreover, the manufacture approach (claim 12) of other semiconductor devices concerning this invention is characterized by said heat treatment being what performs formation of said rearrangement defective field, and induction of said distortion to coincidence in the manufacture approach (claim 8) of the above-mentioned semiconductor device.
[0022] Moreover, the manufacture approach (claim 13) of other semiconductor devices concerning this invention is characterized by being the ion of at least one element chosen from the element group which said ion becomes from a hydrogen element and an inactive element in the manufacture approach (claim 8 - claim 12) of the above-mentioned semiconductor device.

[Translation done.]

* NOTICES *

OPERATION

A base [operation] this invention view has the 1st semi-conductor layer, an insulating layer, and the 2nd semi-conductor layer in using the substrate (SOI substrate) which comes to carry out a laminating one by one, in order to obtain a distortion semi-conductor layer.
[0024] That is, in this invention, first, ion is injected into the 1st semi-conductor layer, and a rearrangement defective field is formed in the 1st semi-conductor layer by heat treatment. A rearrangement defective field can separate the 1st semi-conductor layer and insulating layer in stress.
[0025] Thus, if the 1st semi-conductor layer and insulating layer lower the 2nd semi-conductor layer and insulating layer to a room temperature from a hot (preferably beyond the viscous flow temperature of an insulating layer) condition in the condition of having dissociated in stress, the 2nd semi-conductor layer and insulating layer will come to receive distortion decided by both coefficient of thermal expansion and thickness.
[0026] Here, although a coefficient of thermal expansion is unchangeable, since thickness is changeable, sufficient distortion for the 2nd semi-conductor layer can be generated by adjusting the 2nd semi-conductor layer and insulating layer thickness.
[0027] Thus, according to this invention, sufficient hauling distortion for the 2nd semi-conductor layer can be produced by the ion implantation and heat treatment. Namely, a distortion semi-conductor layer can be easily formed now, without using a highly precise epitaxial growth system and a process technique.
[0028] Moreover, in this invention, although a rearrangement defective field is formed, since the insulating layer dissociates with the 2nd semi-conductor layer, a rearrangement defect does not generate this rearrangement defective field in the 2nd semi-conductor layer. Namely, a reliable distortion semi-conductor layer can be formed now.
[0029] Therefore, according to this invention, it can be reliable and the semi-conductor layer which has sufficient hauling distortion can be easily formed now. The semiconductor device (claim 1) concerning this invention is the thing of most fundamental configuration of that offer of a reliable distortion semi-conductor layer is attained.
[0030] Moreover, the characteristic configuration (rearrangement defective field) produced in case the semiconductor device (claim 2) concerning this invention manufactures the above-mentioned semiconductor device (claim 1) is added. Moreover, the semiconductor device (claim 3) concerning this invention limits the location of the most desirable rearrangement defective field, in order to obtain sufficient distortion.
[0031] Moreover, the semiconductor device (claim 4) concerning this invention limits the typical value of a rearrangement defective field in case the principal component of the 1st semi-conductor layer is silicon. Moreover, the semiconductor device (claim 5) concerning this invention limits the size relation between the thickness of the 2nd semi-conductor layer effective in obtaining sufficient distortion, and that of an insulating layer.
[0032] moreover, the case where the principal component of the 2nd semi-conductor layer of the semiconductor device (claim 6) concerning this invention is silicon -- this -- the value of the typical tensile stress, from which the 2nd semi-conductor layer is obtained is limited.
[0033] Moreover, for the principal component of the 2nd semi-conductor layer, the principal

component of silicon and an insulating layer is [the semiconductor device (claim 7) concerning this invention] SiO2. The size relation between the thickness of the 2nd semi-conductor layer effective in obtaining sufficient distortion and that of an insulating layer is limited to a case.
[0034] Moreover, the manufacture approach (claim 8) of the semiconductor device concerning this invention is the thing of most fundamental configuration of that offer of a reliable distortion semi-conductor layer is attained. Moreover, the manufacture approach (claim 9) of the semiconductor device concerning this invention limits having divided into the 1st heat treatment for forming a rearrangement defective field for heat treatment, and the 2nd heat treatment for making the 2nd semi-conductor layer generate distortion in the manufacture approach (claim 8) of the above-mentioned semiconductor device.
[0035] Moreover, the manufacture approach (claim 10) of the semiconductor device concerning this invention limits the desirable temperature of the 2nd heat treatment. Moreover, for the manufacture approach (claim 11) of the semiconductor device concerning this invention, the principal component of an insulating layer is SiO2. The desirable temperature of the 2nd heat treatment of a case is limited.
[0036] Moreover, the manufacture approach (claim 12) of the semiconductor device concerning this invention limits managing one heat treatment in the manufacture approach (claim 8) of the above-mentioned semiconductor device, without dividing into heat treatment for forming a rearrangement defective field, and heat treatment for making the 2nd semi-conductor layer generate distortion. Moreover, the manufacture approach (claim 13) of the semiconductor device concerning this invention limits ion effective in forming a rearrangement defective field.
[0037]
[Embodiment of the Invention] Hereafter, the gestalt (henceforth an operation gestalt) of operation of this invention is explained, referring to a drawing.
(1st operation gestalt) Drawing 1 is the process sectional view showing the formation approach of MOSFET concerning the 1st operation gestalt of this invention.
[0038] First, as shown in drawing 1 (a), they are the 1st silicon layer 1 as a support substrate, and SiO2. A layer 2 and the 2nd silicon layer 3 as a barrier layer in which a component is formed prepare the SOI substrate which comes to carry out a laminating one by one.
[0039] The thickness of the 1st silicon layer 1 is 700 micrometers and SiO2. The thickness of 100 micrometers and the 2nd silicon layer 3 of the thickness of a layer 2 is 20 micrometers. Thus, for the usual SOI substrate, the SOI substrates of this operation gestalt differ and the 2nd silicon layer 3 is SiO2. It is thinner than a layer 2. This is for heightening the effectiveness of this invention mentioned later. The thickness of the 2nd silicon layer 3 is SiO2 like this operation gestalt. It is desirable that it is 1/5 or less [of the thickness of a layer 2].
[0040] As the formation approach of a SOI substrate, after injecting oxygen ion into a silicon layer, any usual approach, such as the approach (SIMOX law) of performing annealing and forming a silicon oxidizing zone and the approach (lamination method) of making the silicon layer of two sheets rival through a silicon oxidizing zone, and forming it, may be used.
[0041] Next, as shown in drawing 1 (b), it is 2 acceleration voltage 20keV and 1x1016 doses/cm. On conditions, a hydrogen ion is injected into the 1st silicon layer 1 from the 2nd silicon layer 3 side. Thereby, a hydrogen ion is the 1st silicon layer 1 and SiO2. It is introduced into the 1st silicon layer [/ near the interface with a layer 2] 1.
[0042] In addition, the ion of an inactive element may be poured in instead of a hydrogen ion. As ion, a hydrogen ion and the ion of an inactive element are used because these ion is effective in formation of a rearrangement defect.
[0043] Next, as shown in this drawing (b), the 1st annealing with a temperature of about 400-600 degrees C is performed, and it is the 1st silicon layer 1 and SiO2. In the 1st [near the interface with a layer 2] silicon layer 1, the consistency of a rearrangement defect is 2 about 1x1015 pieces/cm. The rearrangement defective field 5 is formed. By this rearrangement defective field 5, it is the 1st silicon layer 1 and SiO2. It dissociates in [a layer 2] stress.
[0044] The consistency of the defect is small and seems in addition, not to form a defective field like this operation gestalt in the usual SOI substrate, although a defect exists in the silicon layer by the side of an insulator layer.

[0045] Then, SiO2 The 2nd with a viscous flow temperature [of a layer 2 / beyond] (900 degrees C), for example, about 950-degree C temperature, annealing is performed, it pulls in the 2nd silicon layer 3, and distortion is generated. The SOI substrate which pulls in this phase and has distortion is completed.
[0046] The reason which pulls in the 2nd silicon layer 3 and distortion generates is as follows. SiO2 Above the viscous flow temperature of a layer 2, it is SiO2. The stress of a layer 2 and the 2nd silicon layer 3 is eased.
[0047] and -- if temperature falls even from the high temperature beyond viscous flow temperature to a room temperature -- SiO two-layer -- the 2 and 2nd silicon layers 3 will take charge of distortion decided by both coefficient of thermal expansion and thickness, respectively.

[0048] Specifically, it is SiO2. Since a coefficient of thermal expansion is 4.0x10-6/degree C, 0.4x10-6/degree C and the number of thermal-expansion formation of silicon For example, SiO2 Hauling distortion from which the thickness of a layer 2 will become 1.01 or more times of the lattice constant of original [lattice constant / of the silicon in the 2nd silicon layer 3] of silicon if the thickness of 100nm and the 2nd silicon layer 3 is 20nm occurs in the 2nd silicon layer 3.
[0049] Generally hauling distortion generated in the 2nd silicon layer 3 is SiO2. It becomes so large that the 2nd silicon layer 3 is so thin that the thickness of a layer 2 is thick. Then, in order to generate tensile stress sufficient with this operation gestalt for the 2nd silicon layer 3, as it mentioned above, the usual SOI substrates differ, and it is the thickness of the 2nd silicon layer 3 SiO2 It is made smaller than that of a layer 2.
[0050] To Table 1, it is SiO2. The value of the hauling distortion in the thickness (Si thickness) of the 2nd typical silicon layer 3 in case the thickness of a layer 2 is 100nm is shown. The percentage to an original lattice constant has shown hauling distortion. The thickness of the 2nd silicon layer 3 is SiO2 from a table. About [of the thickness of a layer 2 / 1/5 or less], it turns out that sufficient hauling distortion of about 1% is obtained.
[0051]
[Table 1]

Si膜厚 (nm)	引っ張り歪み (%)
100	0.032
80	0.035
60	0.042
40	0.062
20	0.117

(SiO_2 膜厚：100nm)

[0052] Here, if the rearrangement defective field 5 does not exist that is, it is the 1st silicon layer 1 and SiO2. If the layer 2 is not separated in stress, since the 1st silicon layer 1 of overwhelming thickness (700 micrometers) will govern the whole, it is SiO2. Although a layer 2 receives a big distortion, the 2nd silicon layer 2 hardly receives distortion.
[0053] In addition, you may make it the 1st annealing serve as the 2nd annealing by making temperature of the 1st annealing into 950 degrees C. Next, as shown in drawing 1 (c), isolation is performed by processing the 2nd silicon layer 3 into island shape, and embedding and forming the isolation insulator layer 6 in the perimeter. Next, as shown in this drawing (c), p mold impurity is introduced into the 2nd silicon layer 3, and a threshold electrical potential difference is adjusted.
[0054] Next, as shown in drawing 1 (d), after forming gate oxide 7 in the whole surface, the gate electrode 8 which consists of polycrystalline silicon is formed. Finally, by the ion implantation of n mold impurity which used the gate electrode 8 for the mask, the source drain diffusion layer 9 is formed in self align, and basic structure is completed.
[0055] After this, processes, such as a deposition process of an interlayer insulation film, a puncturing process of a contact hole, and a formation process of a source drain electrode, as well as the process of the usual MOSFET continue.

[0056] As stated above, according to the formation approach of this operation gestalt, sufficient hauling distortion for the 2nd silicon layer 3 can be produced by the ion implantation in the process of drawing 1 (b), and annealing of the 1st and 2 **. Namely, a distortion silicon layer can be easily formed now, without using a highly precise epitaxial growth system and a process technique.
[0057] Moreover, although the rearrangement defective field 5 is formed by the formation approach of this operation gestalt, this rearrangement defective field 5 is SiO2. By the layer 2, since it dissociates in the 2nd silicon layer 3, a rearrangement defect does not occur in the 2nd silicon layer 3. Namely, a reliable distortion silicon layer can be formed now.
[0058] Therefore, according to this operation gestalt, it can be reliable and the silicon layer 3 which has sufficient hauling distortion can be easily formed now. Moreover, a channel is formed in the silicon layer 3 which has sufficient hauling distortion in MOSFET of this operation gestalt. Generally, in the large distortion silicon layer of hauling distortion, an electronic effective mass becomes small.
[0059] Therefore, according to this operation gestalt, high MOSFET of current drive capacity can be realized now. For example, if the large distortion silicon layer of hauling distortion is used, compared with the case where an undistorted silicon layer is used, the component of the current drive capacity to be twice [about] many as this is realizable as reported to "International Electron Device Conference 1944 proceedings."
[0060] Moreover, as mentioned above, since the dependability without a rearrangement defect of the silicon layer 3 (component formation field) is high, only high current drive capacity is not only realizable, but it can realize stable high current drive capacity.
[0061] In addition, this invention is not limited to the above-mentioned operation gestalt. For example, although the above-mentioned operation gestalt explained the case where this invention was applied to MOSFET, this invention is applicable to other semiconductor devices, for example, a bipolar transistor. The sectional view of the bipolar transistor which applied this invention to drawing 2 is shown. Among drawing, in 11, n mold collector layer and 12 show p mold base layer, and 13 shows n mold emitter layer.
[0062] Moreover, since current drive capacity is high, semiconductor devices which applied this invention, such as MOSFET and a bipolar transistor, are effective as a configuration component of a logical circuit, for example.
[0063] moreover — the above-mentioned operation gestalt — the principal component of a semi-conductor layer — the principal component of silicon and an insulating layer — SiO2 it is — although the case where it was a SOI substrate was explained, this invention is applicable also to the SOI (Semiconductor On Insulator) substrate of other ingredient systems. In addition, in the technical range of this invention, it deforms variously and can carry out.

[Translation done.]

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] The process sectional view showing the formation approach of MOSFET concerning the 1st operation gestalt of this invention
[Drawing 2] The sectional view showing the bipolar transistor which applied this invention
[Drawing 3] The sectional view showing the substrate which has the conventional distortion silicon layer
[Description of Notations]
1 — 1st silicon layer (1st semi-conductor layer)
2 — SiO2 Layer
3 — 2nd silicon layer (2nd semi-conductor layer)
4 — Ion
5 — Rearrangement defective field
6 — Isolation insulator layer
7 — Gate oxide
8 — Gate electrode
9 — n mold source drain diffusion layer
11 — n mold collector layer
12 — p mold base layer
13 — n mold emitter layer

[Translation done.]

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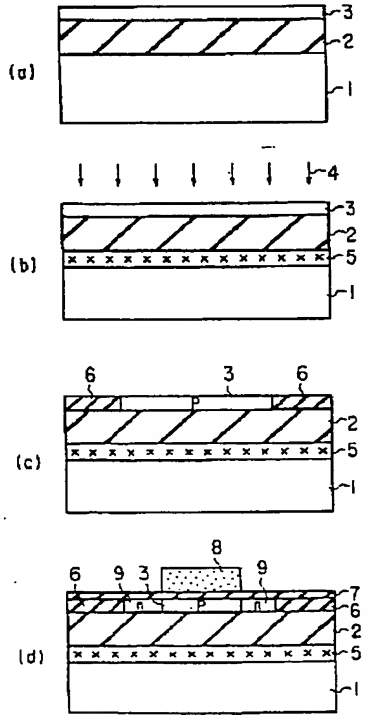
(54)【発明の名称】　半導体装置およびその製造方法

(57)【要約】
【課題】転位欠陥の発生を招かず、かつ簡単な方法で歪みシリコン層を形成すること。
【解決手段】まず、第１のシリコン層１、SiO_2 層２、第２のシリコン層３が順次積層してなるＳＯＩ基板を用意し、次に第１のシリコン層１にイオン４を注入した後、第１のアニールにより第１のシリコン層１内に転位欠陥領域５を形成して、第１のシリコン層１とSiO_2 層２を応力的に分離し、次にSiO_2 の粘性流動温度以上の第２のアニールにより第２のシリコン層２に引っ張り歪みを発生させる。



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【特許請求の範囲】

【請求項１】第１の半導体層、絶縁層、第２の半導体層が順次積層されてなる基板を具備してなり、前記第２の半導体層には歪みが入っており、かつ素子が形成されていることを特徴とする半導体装置。

【請求項２】前記第１の半導体層内に転位欠陥領域が形成されていることを特徴とする請求項１に記載の半導体装置。

【請求項３】前記転位欠陥領域は、前記第１の半導体層と前記絶縁層との界面に形成されていることを特徴とする請求項２に記載の半導体装置。

【請求項４】前記第１の半導体層はシリコンを主成分とし、かつ前記転位欠陥領域の転位欠陥の密度は1×10^{10}個／cm^2以上であることを特徴とする請求項２または請求項３に記載の半導体装置。

【請求項５】前記第２の半導体層の厚さが、前記絶縁層の厚さより小さいことを特徴とする請求項１ないし請求項４のいずれかに記載の半導体装置。

【請求項６】前記第２の半導体層はシリコンを主成分とし、かつ前記歪みは、前記第２の半導体層中における前記シリコンの格子定数が、シリコンの本来の格子定数の１．０１倍以上となる引っ張り歪みであることを特徴とする請求項１ないし請求項４のいずれかに記載の半導体装置。

【請求項７】前記第２の半導体層はシリコンを主成分とし、前記絶縁層はSiO_2を主成分とし、かつ前記第２の半導体層の厚さが、前記絶縁層の厚さの１／５以下であることを特徴とする請求項１ないし請求項４のいずれかに記載の半導体装置。

【請求項８】第１の半導体層、絶縁層、第２の半導体層が順次積層されてなる基板を用意し、前記第１の半導体層にイオンを注入する工程と、

熱処理により、前記イオンに基づいた転位欠陥領域を前記第１の半導体層内に形成して、前記第１の半導体層と前記絶縁層を応力的に分離するとともに、前記第２の半導体層に歪みを発生させる工程と、

前記第２の半導体層に素子を形成する工程とを有することを特徴とする半導体装置の製造方法。

【請求項９】前記熱処理は、前記転位欠陥領域を形成する第１の熱処理と、この第１の熱処理の後に行なわれ、前記歪みを発生させる第２の熱処理とから構成されていることを特徴する請求項８に記載の半導体装置の製造方法。

【請求項１０】前記第２の熱処理の温度は、前記絶縁層の粘性流動温度以上であることを特徴する請求項９に記載の半導体装置の製造方法。

【請求項１１】前記絶縁層はSiO_2を主成分とし、かつ前記温度は９００℃以上であることを特徴する請求項１０に記載の半導体装置の製造方法。

【請求項１２】前記熱処理は、前記転位欠陥領域の形成および前記歪みの誘起を同時に行なうものであることを特徴とする請求項８に記載の半導体装置の製造方法。

【請求項１３】前記イオンは、水素元素および不活性元素からなる元素群から選ばれた少なくとも１つの元素のイオンであることを特徴とする請求項８ないし請求項１２のいずれかに記載の半導体装置の製造方法。

【発明の詳細な説明】

【０００１】

【発明の属する技術分野】本発明は、歪みの入った半導体層に素子を形成した半導体装置およびその製造方法に関する。

【０００２】

【従来の技術】コンピューターや通信機器の重要部分には、多数のトランジスタや抵抗等を電気回路を達成するようにむすびつけ、１チップ上に集積化して形成した大規模集積回路（ＬＳＩ）が多用されている。このため、機器全体の性能は、ＬＳＩ単体の性能と大きく結び付いている。

【０００３】ＬＳＩ単体の性能向上、例えば、Ｓｉ系ＭＯＳデバイス等で構成されるＬＳＩ単体の性能向上においては、高速かつ低消費電力を特徴とするＭＯＳＦＥＴの実現が不可欠である。このため、例えば、電流駆動力等の電気的特性の向上を目的とした研究開発が精力的に行なわれている。

【０００４】電流駆動力を高めるための技術の１つとして、歪みの入ったシリコン層（歪みシリコン層）に素子を形成する技術が知られている。図３に、従来の歪みシリコン層を有する基板の断面図を示す。

【０００５】図中、８１はシリコン基板を示しており、このシリコン基板８１上には、グレーテッドＳｉＧｅ混晶層８２、緩和ＳｉＧｅ混晶層８３、歪みシリコン層８４が順次形成されている。この種の基板では、グレーテッドＳｉＧｅ混晶層８２内に転位欠陥が閉じ込められ、緩和ＳｉＧｅ混晶層８３には転位欠陥が入らないとされている。

【０００６】

【発明が解決しようとする課題】しかしながら、実際には、緩和ＳｉＧｅ混晶層８３にまで転位欠陥が入り、さらにこの転位欠陥は歪みシリコン層８４にまで達してしまう。したがって、この転位欠陥により、歪みシリコン層８４の信頼性が低下するため、歪みシリコン層８４に素子を形成しても、期待通りの電気的特性を得ることが困難であるという問題があった。

【０００７】さらに、グレーテッドＳｉＧｅ混晶層８２、緩和ＳｉＧｅ混晶層８３を形成するためには、高精度のエピタキシャル成長装置およびプロセス技術が必要であるので、歪みシリコン層８４を容易に形成することが困難であるという問題があった。

【０００８】上述の如く、歪みシリコン層は、電流駆動力等の素子特性の向上に有効であるが、転位欠陥の発生

を招くことなく、容易に形成することが困難であるという問題があった。

【０００９】本発明は上記事情を考慮してなされたもので、その目的とするところは、歪み半導体層を含み、かつ該歪み半導体層をその内部に転位欠陥の発生を招くことなく、容易に形成することができる基板を備えた半導体装置およびその製造方法を提供することにある。

【００１０】

【課題を解決するための手段】

［概要］上記目的を達成するために、本発明に係る半導体装置（請求項１）は、第１の半導体層、絶縁層、第２の半導体層が順次積層されてなる基板を具備してなり、前記第２の半導体層には歪みが入っており、かつ素子が形成されていることを特徴とする。

【００１１】また、本発明に係る他の半導体装置（請求項２）は、上記半導体装置（請求項１）において、前記第１の半導体層内に転位欠陥領域が形成されていることを特徴とする。

【００１２】また、本発明に係る他の半導体装置（請求項３）は、上記半導体装置（請求項２）において、前記転位欠陥領域が、前記第１の半導体層と前記絶縁層との界面に形成されていることを特徴とする。

【００１３】また、本発明に係る他の半導体装置（請求項４）は、上記半導体装置（請求項２、請求項３）において、前記第１の半導体層がシリコンを主成分とし、かつ前記転位欠陥領域の転位欠陥の密度が1×10^{10}個／cm^2以上であることを特徴とする。

【００１４】また、本発明に係る他の半導体装置（請求項５）は、上記半導体装置（請求項１～請求項４）において、前記第２の半導体層の厚さが、前記絶縁層の厚さより小さいことを特徴とする。

【００１５】また、本発明に係る他の半導体装置（請求項６）は、上記半導体装置（請求項１～請求項４）において、前記第２の半導体層がシリコンを主成分とし、かつ前記歪みが、前記第２の半導体層中における前記シリコンの格子定数が、シリコンの本来の格子定数の１．０１倍以上となる引っ張り歪みであることを特徴とする。

【００１６】また、本発明に係る他の半導体装置（請求項７）は、上記半導体装置（請求項１～請求項４）において、前記第２の半導体層がシリコンを主成分とし、前記絶縁層がSiO_2を主成分とし、かつ前記第２の半導体層の厚さが、前記絶縁層の厚さの１／５以下であることを特徴とする。

【００１７】また、本発明に係る半導体装置の製造方法（請求項８）は、第１の半導体層、絶縁層、第２の半導体層が順次積層されてなる基板を用意し、前記第１の半導体層にイオンを注入する工程と、熱処理により、前記イオンに基づいた転位欠陥領域を前記第１の半導体層内に形成して、前記第１の半導体層と前記絶縁層を応力的に分離するとともに、前記第２の半導体層に歪みを発生させる工程と、前記第２の半導体層に素子を形成する工程とを有することを特徴とする。

【００１８】また、本発明に係る他の半導体装置の製造方法（請求項９）は、上記半導体装置の製造方法（請求項８）において、前記熱処理が、前記転位欠陥領域を形成する第１の熱処理と、この第１の熱処理の後に行なわれ、前記歪みを発生させる第２の熱処理とから構成されていることを特徴する。

【００１９】また、本発明に係る他の半導体装置の製造方法（請求項１０）は、上記半導体装置の製造方法（請求項９）において、前記第２の熱処理の温度が、前記絶縁層の粘性流動温度以上であることを特徴する。

【００２０】また、本発明に係る他の半導体装置の製造方法（請求項１１）は、上記半導体装置の製造方法（請求項１０）において、前記絶縁層がSiO_2を主成分とし、かつ前記温度が９００℃以上であることを特徴する。

【００２１】また、本発明に係る他の半導体装置の製造方法（請求項１２）は、上記半導体装置の製造方法（請求項８）において、前記熱処理が、前記転位欠陥領域の形成および前記歪みの誘起を同時に行なうものであることを特徴とする。

【００２２】また、本発明に係る他の半導体装置の製造方法（請求項１３）は、上記半導体装置の製造方法（請求項８～請求項１２）において、前記イオンが、水素元素および不活性元素からなる元素群から選ばれた少なくとも１つの元素のイオンであることを特徴とする。

【００２３】［作用］本発明の基本な考え方は、歪み半導体層を得るために、第１の半導体層、絶縁層、第２の半導体層が順次積層されてなる基板（ＳＯＩ基板）を利用することにある。

【００２４】すなわち、本発明では、まず、第１の半導体層にイオンを注入し、熱処理により第１の半導体層内に転位欠陥領域を形成する。転位欠陥領域は第１の半導体層と絶縁層を応力的に分離することができる。

【００２５】このように第１の半導体層と絶縁層が応力的に分離された状態で、第２の半導体層および絶縁層を高温（好ましくは絶縁層の粘性流動温度以上）の状態から室温に下げると、第２の半導体層および絶縁層は、両者の熱膨張係数および厚さで決まる歪みを受けるようになる。

【００２６】ここで、熱膨張係数を変えることはできないが、厚さを変えることはできるので、第２の半導体層および絶縁層の厚さを調整することにより、第２の半導体層に十分な歪みを発生させることができる。

【００２７】このように本発明によれば、イオン注入と熱処理により、第２の半導体層に十分な引っ張り歪みを生じさせることができる。すなわち、高精度のエピタキシャル成長装置やプロセス技術を用いずに、歪み半導体層を容易に形成できるようになる。

【００２８】また、本発明では、転位欠陥領域を形成するが、この転位欠陥領域は絶縁層により、第２の半導体層とは分離されているので、第２の半導体層に転位欠陥が発生することはない。すなわち、信頼性の高い歪み半導体層を形成できるようになる。

【００２９】したがって、本発明によれば、信頼性が高く、十分な引っ張り歪みを有する半導体層を容易に形成できるようになる。本発明に係る半導体装置（請求項１）は、信頼性の高い歪み半導体層の提供が可能となる最も基本的な構成のものである。

【００３０】また、本発明に係る半導体装置（請求項２）は、上記半導体装置（請求項１）を製造する際に生じる特徴ある構成（転位欠陥領域）が追加されたものである。また、本発明に係る半導体装置（請求項３）は、十分な歪みを得るために最も好ましい転位欠陥領域の位置を限定したものである。

【００３１】また、本発明に係る半導体装置（請求項４）は、第１の半導体層の主成分がシリコンの場合の転位欠陥領域の典型的な値を限定したものである。また、本発明に係る半導体装置（請求項５）は、十分な歪みを得るのに有効な第２の半導体層の厚さと絶縁層のそれとの大小関係を限定したものである。

【００３２】また、本発明に係る半導体装置（請求項６）は、第２の半導体層の主成分がシリコンの場合に、該第２の半導体層が得られる典型的な引っ張り応力の値を限定したものである。

【００３３】また、本発明に係る半導体装置（請求項７）は、第２の半導体層の主成分がシリコン、絶縁層の主成分がSiO_2の場合に、十分な歪みを得るのに有効な第２の半導体層の厚さと絶縁層のそれとの大小関係を限定したものである。

【００３４】また、本発明に係る半導体装置の製造方法（請求項８）は、信頼性の高い歪み半導体層の提供が可能となる最も基本的な構成のものである。また、本発明に係る半導体装置の製造方法（請求項９）は、上記半導体装置の製造方法（請求項８）において、熱処理を転位欠陥領域を形成するための第１の熱処理と、第２の半導体層に歪みを発生させるための第２の熱処理とに分けたことを限定したものである。

【００３５】また、本発明に係る半導体装置の製造方法（請求項１０）は、第２の熱処理の好ましい温度を限定したものである。また、本発明に係る半導体装置の製造方法（請求項１１）は、絶縁層の主成分がSiO_2の場合の第２の熱処理の好ましい温度を限定したものである。

【００３６】また、本発明に係る半導体装置の製造方法（請求項１２）は、上記半導体装置の製造方法（請求項８）において、転位欠陥領域を形成するための熱処理と、第２の半導体層に歪みを発生させるための熱処理とに分けずに、１つの熱処理で済ませることを限定したものである。また、本発明に係る半導体装置の製造方法（請求項１３）は、転位欠陥領域を形成するのに有効なイオンを限定したものである。

【００３７】

【発明の実施の形態】以下、図面を参照しながら本発明の実施の形態（以下、実施形態という）を説明する。

（第１の実施形態）図１は、本発明の第１の実施形態に係るＭＯＳＦＥＴの形成方法を示す工程断面図である。

【００３８】まず、図１（ａ）に示すように、支持基板としての第１のシリコン層１、SiO_2層２、素子が形成される活性層としての第２のシリコン層３が順次積層されてなるＳＯＩ基板を用意する。

【００３９】第１のシリコン層１の厚さは例えば７００μｍ、SiO_2層２の厚さは例えば１００μｍ、第２のシリコン層３の厚さは例えば２０μｍである。このように、本実施形態のＳＯＩ基板は、通常のＳＯＩ基板とは異なり、第２のシリコン層３はSiO_2層２よりも薄い。これは後述する本発明の効果を高めるためである。第２のシリコン層３の厚さは、本実施形態のように、SiO_2層２の厚さの１／５以下であることが好ましい。

【００４０】ＳＯＩ基板の形成方法としては、シリコン層に酸素イオンを注入した後にアニールを行なってシリコン酸化層を形成する方法（ＳＩＭＯＸ法）や、２枚のシリコン層をシリコン酸化層を介して張り合わせて形成する方法（張り合わせ法）等の通常のどの方法を用いても良い。

【００４１】次に図１（ｂ）に示すように、加速電圧２０ｋｅＶ、ドーズ量1×10^{16}個／cm^2の条件で、第２のシリコン層３側から第１のシリコン層１に水素イオンを注入する。これにより、水素イオンは、第１のシリコン層１とSiO_2層２との界面近傍における第１のシリコン層１に導入される。

【００４２】なお、水素イオンの代わりに、不活性元素のイオンを注入しても良い。イオンとして、水素イオン、不活性元素のイオンを用いるのは、これらイオンが転位欠陥の形成に有効であるからである。

【００４３】次に同図（ｂ）に示すように、４００～６００℃程度の温度の第１のアニールを行なって、第１のシリコン層１とSiO_2層２との界面近傍の第１のシリコン層１内に、転位欠陥の密度が約1×10^{15}個／cm^2の転位欠陥領域５を形成する。この転位欠陥領域５によって、第１のシリコン層１とSiO_2層２とは応力的に分離される。

【００４４】なお、通常のＳＯＩ基板においても、絶縁膜側のシリコン層に欠陥は存在するが、その欠陥の密度は小さく、本実施形態のような欠陥領域を形成するようなものではない。

【００４５】この後、SiO_2層２の粘性流動温度（９００℃）以上、例えば９５０℃程度の温度の第２のアニールを行なって、第２のシリコン層３に引っ張り歪みを

発生させる。この段階で引っ張り歪を有するＳＯＩ基板が完成する。

【００４６】第２のシリコン層３に引っ張り歪みが発生する理由は以下の通りである。SiO_2 層２の粘性流動温度以上では、SiO_2 層２および第２のシリコン層３の応力は緩和している。

【００４７】そして、粘性流動温度以上の高温度から室温にまで温度が下がると、SiO_2層２および第２のシリコン層３は、両者の熱膨張係数および膜厚で決まる歪みをそれぞれ受け持つことになる。

【００４８】具体的には、SiO_2 の熱膨張係数は０．４×10^{-6}／℃、シリコンの熱膨張形成数は４．０×10^{-6}／℃であるので、例えば、SiO_2 層２の厚さが１００ｎｍ、第２のシリコン層３の厚さが２０ｎｍであれば、第２のシリコン層３中のシリコンの格子定数が、シリコンの本来の格子定数の１．０１倍以上となる引っ張り歪みが第２のシリコン層３に発生する。

【００４９】第２のシリコン層３に発生する引っ張り歪みは、一般に、SiO_2 層２の厚さが厚いほど、第２のシリコン層３が薄いほど大きくなる。そこで、本実施形態では、第２のシリコン層３に十分な引っ張り応力を発生させるために、上述したように、通常のＳＯＩ基板とは異なり、第２のシリコン層３の厚さをSiO_2 層２のそれよりも小さくしている。

【００５０】表１に、SiO_2 層２の厚さが１００ｎｍの場合における、代表的な第２のシリコン層３の厚さ（Ｓｉ膜厚）における引っ張り歪みの値を示す。引っ張り歪みは本来の格子定数に対する百分率で示してある。表から第２のシリコン層３の厚さが、SiO_2 層２の厚さの１／５程度以下では、１％程度の十分な引っ張り歪みが得られることが分かる。

【００５１】

【表１】

Ｓｉ膜厚（ｍｍ）	引っ張り歪み（％）
１００	０．０３２
８０	０．０３５
６０	０．０４２
４０	０．０６２
２０	０．１１７

（SiO_2 膜厚：１００ｎｍ）

【００５２】ここで、転位欠陥領域５が存在しないと、つまり、第１のシリコン層１とSiO_2 層２とが応力的に分離されていないと、圧倒的な厚さ（７００μｍ）の第１のシリコン層１が全体を支配するので、SiO_2 層２は大きな歪みを受けるが、第２のシリコン層２はほとんど歪みを受けない。

【００５３】なお、第１のアニールの温度を例えば９５０℃にすることにより、第１のアニールが第２のアニールを兼ねるようにしても良い。次に図１（ｃ）に示すように、第２のシリコン層３を島状に加工し、その周囲に素子分離絶縁膜６を埋め込み形成することにより、素子分離を行なう。次に同図（ｃ）に示すように、第２のシリコン層３にｐ型不純物を導入して、しきい値電圧の調整を行なう。

【００５４】次に図１（ｄ）に示すように、全面にゲート酸化膜７を形成した後、例えば多結晶シリコンからなるゲート電極８を形成する。最後に、ゲート電極８をマスクに用いたｎ型不純物のイオン注入により、ソース・ドレイン拡散層９を自己整合的に形成して、基本構造が完成する。

【００５５】この後は、通常のＭＯＳＦＥＴのプロセスと同様に、層間絶縁膜の堆積工程、コンタクトホールの開孔工程、ソース・ドレイン電極の形成工程などの工程が続く。

【００５６】以上述べたように、本実施形態の形成方法によれば、図１（ｂ）の工程におけるイオン注入および第１、２第のアニールにより、第２のシリコン層３に十分な引っ張り歪みを生じさせることができる。すなわち、高精度のエピタキシャル成長装置やプロセス技術を用いずに、歪みシリコン層を容易に形成できるようになる。

【００５７】また、本実施形態の形成方法では、転位欠陥領域５を形成するが、この転位欠陥領域５はSiO_2 層２により、第２のシリコン層３とは分離されているので、第２のシリコン層３に転位欠陥が発生することはない。すなわち、信頼性の高い歪みシリコン層を形成できるようになる。

【００５８】したがって、本実施形態によれば、信頼性が高く、十分な引っ張り歪みを有するシリコン層３を容易に形成できるようになる。また、本実施形態のＭＯＳＦＥＴでは、十分な引っ張り歪みを有するシリコン層３にチャネルが形成される。一般に、引っ張り歪みの大きい歪みシリコン層においては、電子の有効質量が小さくなる。

【００５９】したがって、本実施形態によれば、電流駆動能力の高いＭＯＳＦＥＴを実現できるようになる。例えば、引っ張り歪みの大きい歪みシリコン層を用いれば、“International Electron Device Conference 1944 プロシーディングス”に報告されているように、無歪みシリコン層を用いた場合に比べて、約２倍の電流駆動能力の素子を実現することができる。

【００６０】また、上述したように、シリコン層３（素子形成領域）は転位欠陥の無い信頼性の高いものなので、単に高い電流駆動能力を実現できるだけではなく、安定した高い電流駆動能力を実現できるようになる。

【００６１】なお、本発明は上記実施形態に限定されるものではない。例えば、上記実施形態では、本発明をＭ

ＯＳＦＥＴに適用した場合について説明したが、本発明は他の半導体素子、例えばバイポーラトランジスタにも適用できる。図２に、本発明を適用したバイポーラトランジスタの断面図を示す。図中、１１はｎ型コレクタ層、１２はｐ型ベース層、１３はｎ型エミッタ層を示している。

【００６２】また、本発明を適用したＭＯＳＦＥＴやバイポーラトランジスタ等の半導体素子は、電流駆動能力が高いので、例えば、ロジック回路の構成素子として有効である。

【００６３】また、上記実施形態では、半導体層の主成分がシリコン、絶縁層の主成分がSiO_2であるＳＯＩ基板の場合について説明したが、本発明は他の材料系のＳＯＩ(Semiconductor On Insulator)基板にも適用可能である。その他、本発明の技術的範囲で、種々変形して実施できる。

【００６４】

【発明の効果】以上述べたように、本発明によれば、第１の半導体層、絶縁層、第２の半導体層が順次積層されてなる基板（ＳＯＩ基板）を利用することにより、転位欠陥がない歪みシリコン層を容易に得られるようになる。

【図面の簡単な説明】

【図１】本発明の第１の実施形態に係るＭＯＳＦＥＴの形成方法を示す工程断面図

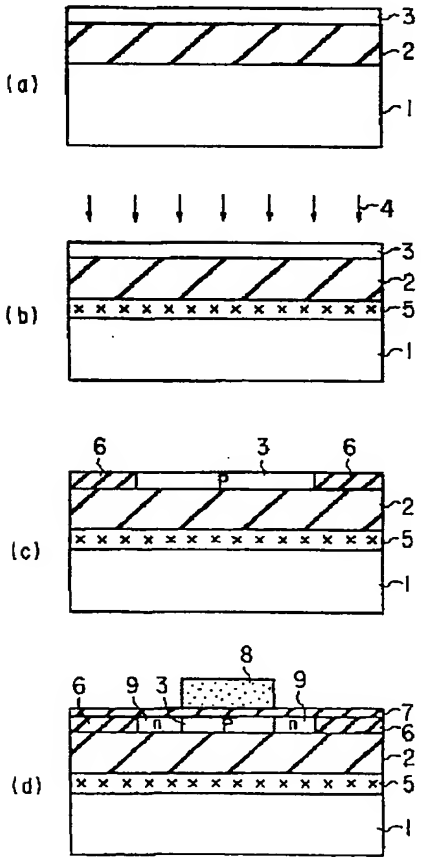
【図２】本発明を適用したバイポーラトランジスタを示す断面図

【図３】従来の歪みシリコン層を有する基板を示す断面図

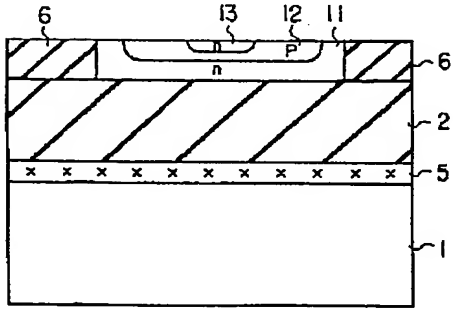
【符号の説明】

１…第１のシリコン層（第１の半導体層）
２…SiO_2層
３…第２のシリコン層（第２の半導体層）
４…イオン
５…転位欠陥領域
６…素子分離絶縁膜
７…ゲート酸化膜
８…ゲート電極
９…ｎ型ソース・ドレイン拡散層
１１…ｎ型コレクタ層
１２…ｐ型ベース層
１３…ｎ型エミッタ層

【図１】



【図２】



【図３】